

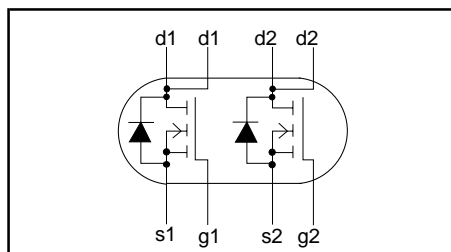
Dual N-channel enhancement mode TrenchMOS™ transistor

PHN203

FEATURES

- Dual device
- Low threshold voltage
- Fast switching
- Logic level compatible
- Surface mount package

SYMBOL



QUICK REFERENCE DATA

| |
|---|
| $V_{DS} = 25 \text{ V}$ |
| $I_D = 6.3 \text{ A}$ |
| $R_{DS(ON)} \leq 30 \text{ m}\Omega (V_{GS} = 10 \text{ V})$ |
| $R_{DS(ON)} \leq 55 \text{ m}\Omega (V_{GS} = 4.5 \text{ V})$ |

GENERAL DESCRIPTION

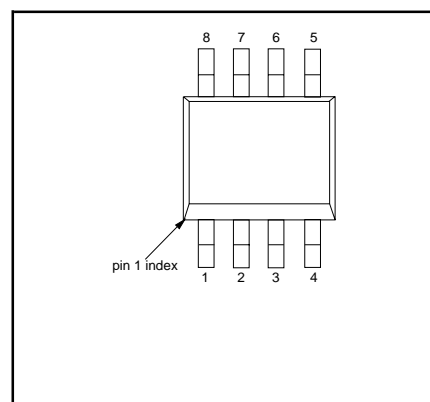
N-channel enhancement mode field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHN203 is supplied in the SOT96-1 (SO8) surface mounting package.

PINNING

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | source 1 |
| 2 | gate 1 |
| 3 | source 2 |
| 4 | gate 2 |
| 5,6 | drain 2 |
| 7,8 | drain 1 |

SOT96-1



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------|--|--|------|----------|------------------|
| V_{DS} | Repetitive peak drain-source voltage | $T_j = 25 \text{ }^\circ\text{C to } 150 \text{ }^\circ\text{C}$ | - | 25 | V |
| V_{DS} | Continuous drain-source voltage | | - | 25 | V |
| V_{DGR} | Drain-gate voltage | $R_{GS} = 20 \text{ k}\Omega$ | - | 25 | V |
| V_{GS} | Gate-source voltage | | - | ± 20 | V |
| I_D | Drain current per MOSFET ¹ | $T_a = 25 \text{ }^\circ\text{C}$ | - | 6.3 | A |
| | | $T_a = 70 \text{ }^\circ\text{C}$ | - | 5 | A |
| I_D | Drain current per MOSFET (both MOSFETs conducting) ¹ | $T_a = 25 \text{ }^\circ\text{C}$ | - | 4.4 | A |
| | | $T_a = 70 \text{ }^\circ\text{C}$ | - | 3.5 | A |
| I_{DM} | Drain current per MOSFET (pulse peak value) | $T_a = 25 \text{ }^\circ\text{C}$ | - | 25 | A |
| P_{tot} | Total power dissipation (either or both MOSFETs conducting) ¹ | $T_a = 25 \text{ }^\circ\text{C}$ | - | 2 | W |
| | | $T_a = 70 \text{ }^\circ\text{C}$ | - | 1.3 | W |
| T_{stg}, T_j | Storage & operating temperature | | - 55 | 150 | $^\circ\text{C}$ |

¹ Surface mounted on FR4 board, $t \leq 10 \text{ sec}$

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THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|---------------|--|--|------|------|------|
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | Surface mounted on FR4 board, $t \leq 10$ sec; either or both MOSFETs conducting | - | 62.5 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | Surface mounted on FR4 board; either or both MOSFETs conducting | 150 | - | K/W |

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------|---|--|------|------|------|
| E_{AS} | Non-repetitive avalanche energy (per MOSFET) | Unclamped inductive load, $I_{AS} = 6.3$ A; $t_p = 0.2$ ms; T_j prior to avalanche = 25°C ; $V_{DD} \leq 15$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V | - | 20 | mJ |
| I_{AS} | Non-repetitive avalanche current (per MOSFET) | | - | 6.3 | A |

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$, per MOSFET unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------|----------------------------------|--|---------------|----------------|-----------------|--|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0$ V; $I_D = 10$ μA ; $T_j = -55^\circ\text{C}$ | 25 22.5 | - - | - - | V V |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 150^\circ\text{C}$ $T_j = -55^\circ\text{C}$ | 1 0.4 - | 2 - - | 2.8 - 3.2 | V V V |
| $R_{DS(ON)}$ | Drain-source on-state resistance | $V_{GS} = 10$ V; $I_D = 4$ A $V_{GS} = 4.5$ V; $I_D = 2$ A $V_{GS} = 10$ V; $I_D = 4$ A; $T_j = 150^\circ\text{C}$ | - - - | 27 40 43 | 30 55 51 | m Ω m Ω m Ω |
| g_{fs} | Forward transconductance | $V_{DS} = 20$ V; $I_D = 4$ A | 5 | 9.7 | - | S |
| I_{DSS} | Zero gate voltage drain current | $V_{DS} = 20$ V; $V_{GS} = 0$ V; $V_{DS} = 20$ V; $V_{GS} = 0$ V; $T_j = 150^\circ\text{C}$ | - - | 60 0.1 | 100 10 | nA μA |
| I_{GSS} | Gate source leakage current | $V_{GS} = \pm 20$ V; $V_{DS} = 0$ V | - | 10 | 100 | nA |
| $Q_{g(tot)}$ | Total gate charge | $I_D = 4$ A; $V_{DD} = 20$ V; $V_{GS} = 10$ V | - | 20 | - | nC |
| Q_{gs} | Gate-source charge | | - | 1.9 | - | nC |
| Q_{gd} | Gate-drain (Miller) charge | | - | 6.1 | - | nC |
| $t_{d\ on}$ | Turn-on delay time | $V_{DD} = 20$ V; $R_D = 18$ Ω ; | - | 8 | - | ns |
| t_r | Turn-on rise time | $V_{GS} = 10$ V; $R_G = 6$ Ω | - | 11 | - | ns |
| $t_{d\ off}$ | Turn-off delay time | Resistive load | - | 31 | - | ns |
| t_f | Turn-off fall time | | - | 17 | - | ns |
| L_d | Internal drain inductance | Measured from drain lead to centre of die | - | 2.5 | - | nH |
| L_s | Internal source inductance | Measured from source lead to source bond pad | - | 5 | - | nH |
| C_{iss} | Input capacitance | $V_{GS} = 0$ V; $V_{DS} = 20$ V; $f = 1$ MHz | - | 611 | - | pF |
| C_{oss} | Output capacitance | | - | 260 | - | pF |
| C_{rss} | Feedback capacitance | | - | 137 | - | pF |

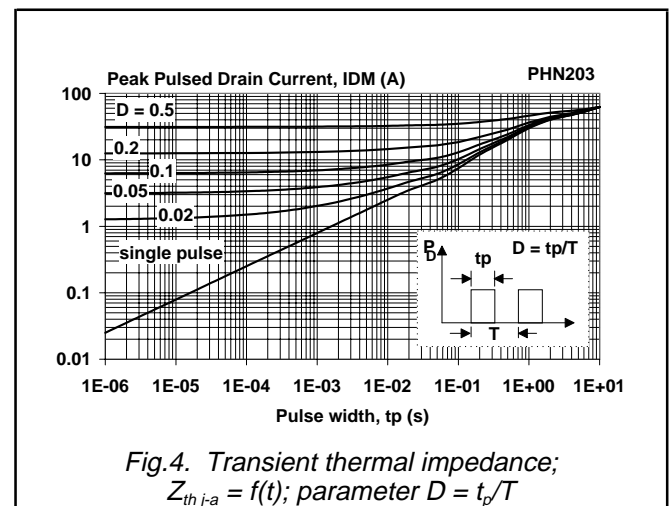
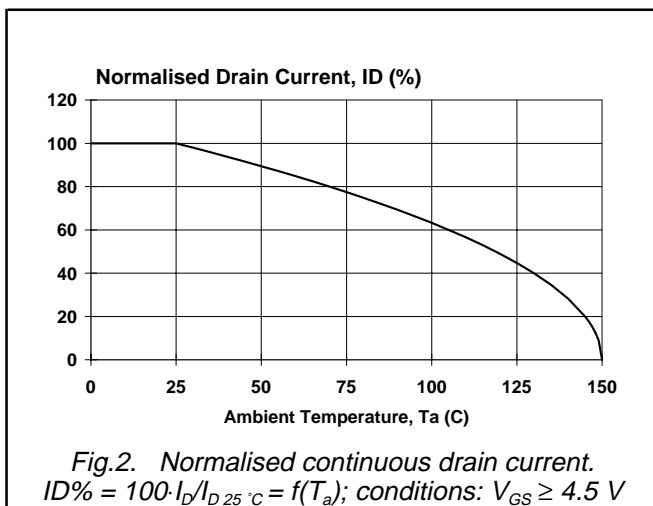
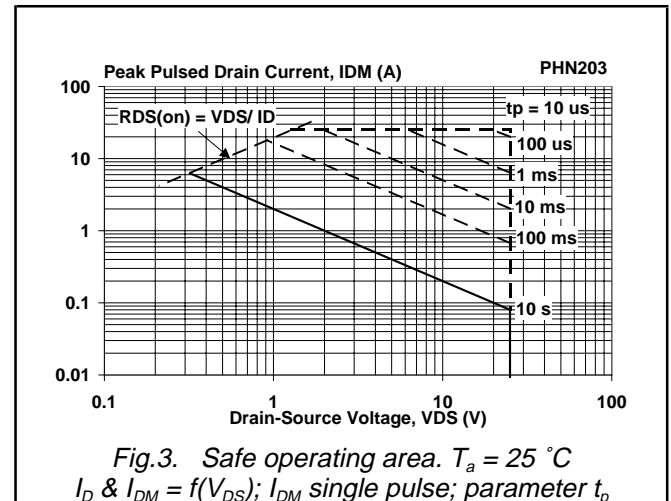
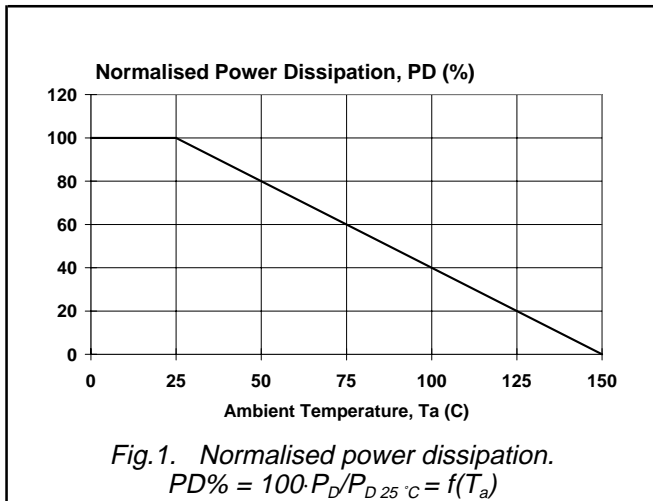
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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

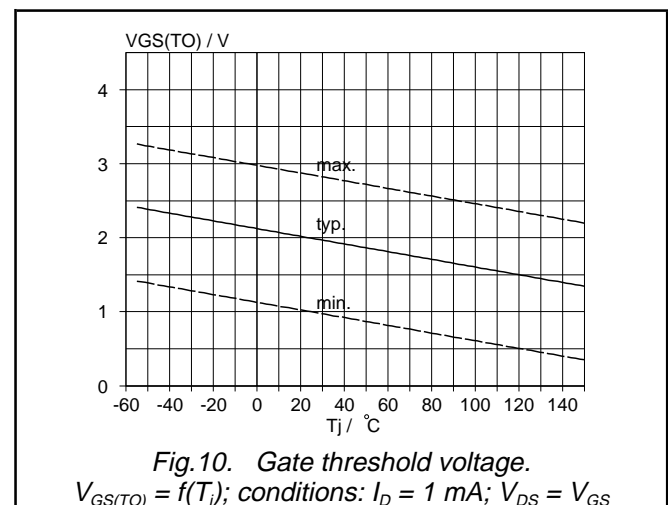
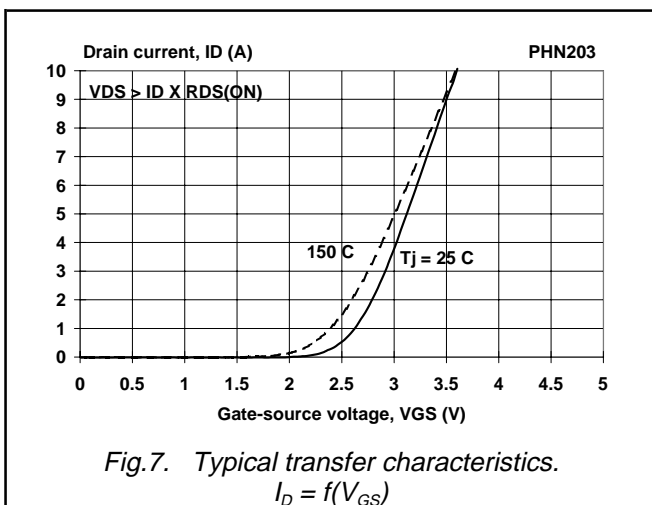
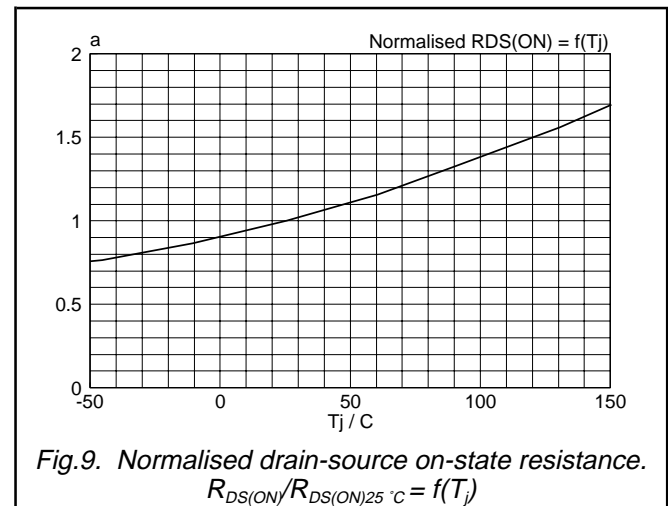
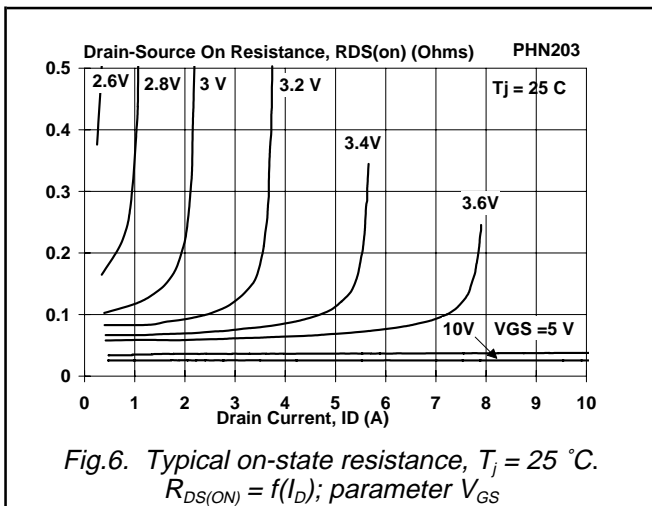
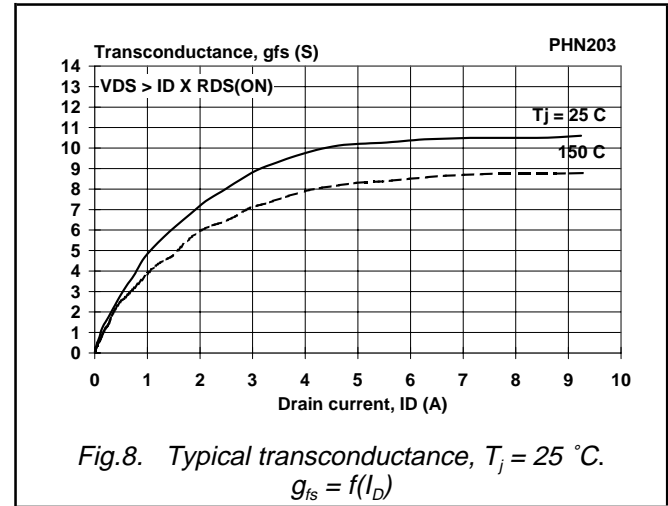
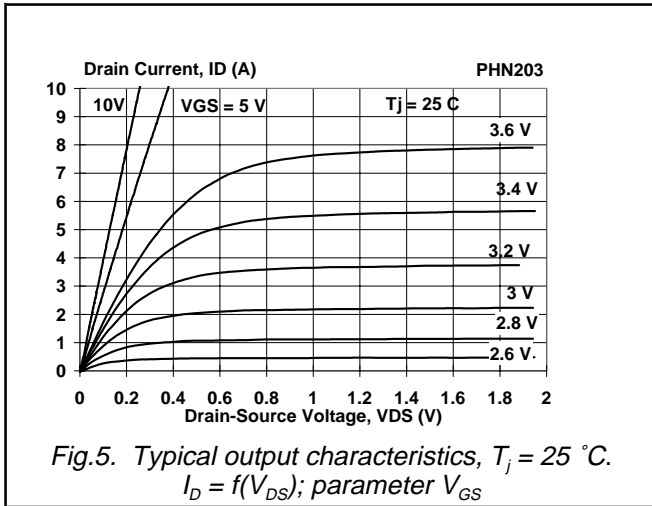
T_j = 25 °C, per MOSFET unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------|--|---|------|------|------|------|
| I _S | Continuous source diode current (per MOSFET) | T _a = 25 °C | - | - | 2.85 | A |
| I _{SM} | Pulsed source diode current (per MOSFET) | | - | - | 25 | A |
| V _{SD} | Diode forward voltage | I _F = 1.25 A; V _{GS} = 0 V | - | 0.75 | 1 | V |
| t _{rr} | Reverse recovery time | I _F = 1.25 A; -di _F /dt = 100 A/μs; | - | 35 | - | ns |
| Q _{rr} | Reverse recovery charge | V _{GS} = 0 V; V _R = 25 V | - | 24 | - | nC |



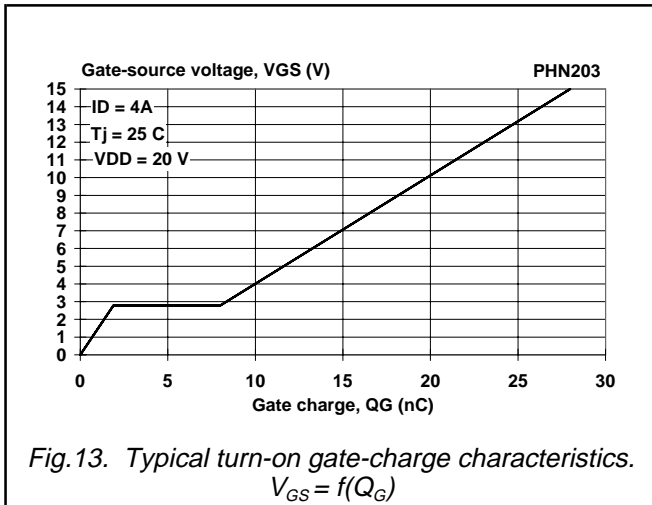
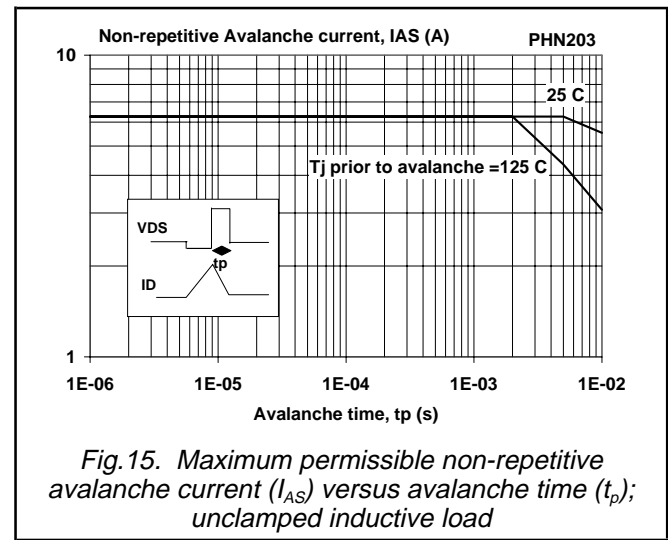
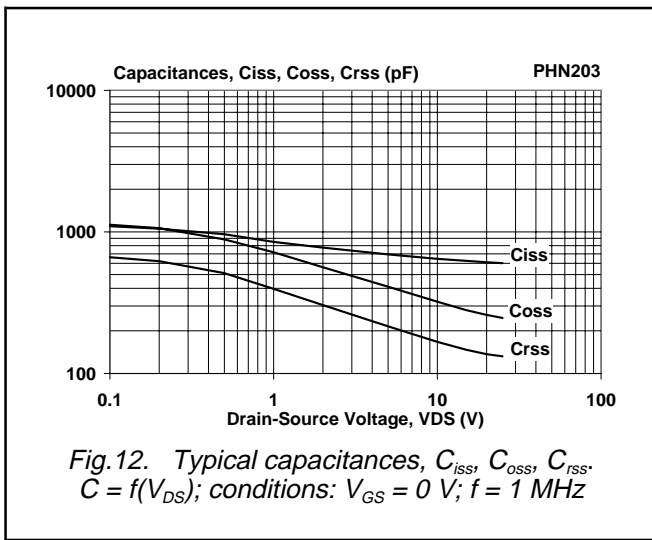
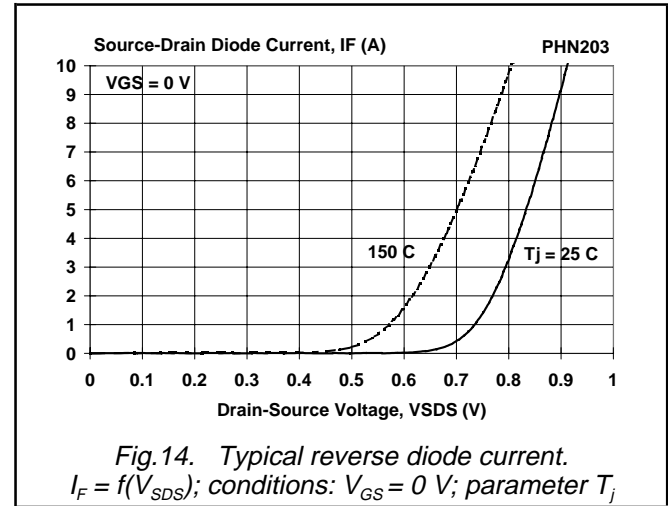
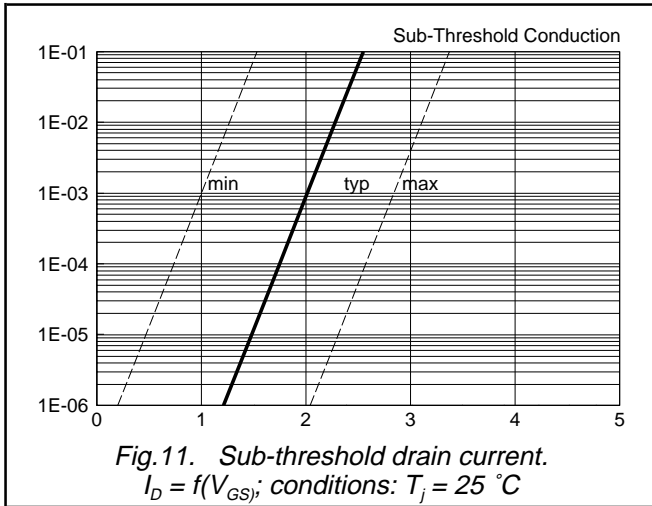
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MECHANICAL DATA

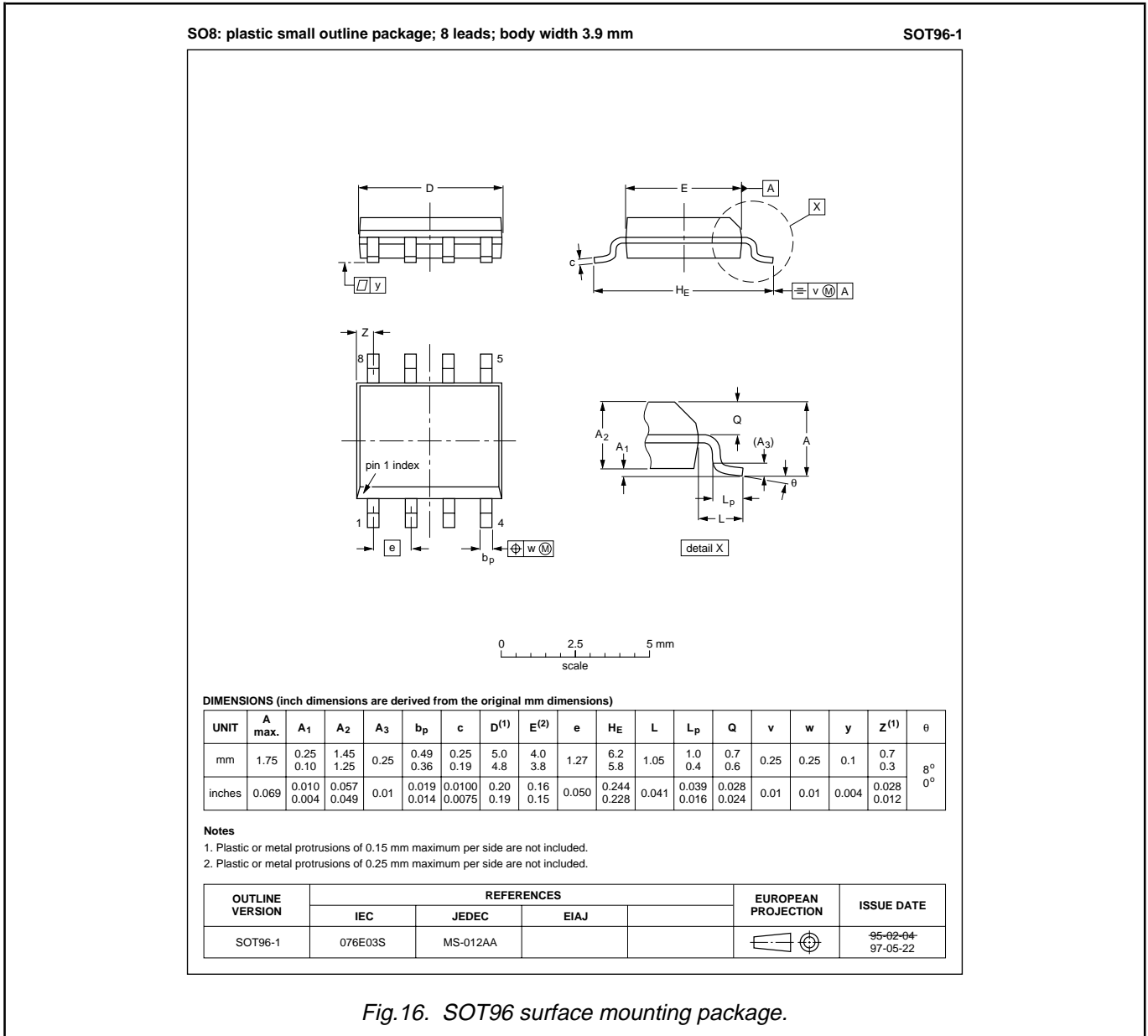


Fig. 16. SOT96 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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